Remarks

Claims 1 - 21 are in the application, of which claims 1 - 13 were withdrawn as being directed to a nonelected invention. Claims 14 - 21 are under consideration. Reconsideration of the application is requested, in view of the following Remarks.

Applicants thank Supervisory Patent Examiner Eddie Lee for his courtesy in responding to a telephone inquiry by Applicant's Representative, undersigned, regarding the status of prosecution of this application; and for his willingness to consider the application himself. In the event it may appear to Examiner Lee that a telephone conference may further prosecution of the application, he is invited to telephone the undersigned at 650 712-0340 to arrange for a telephone interview.

As Applicants understand the status of prosecution, the Office action mailed August 11, 2003 has been WITHDRAWN. The Office action mailed September 10, 2003, replaces the Office action mailed August 11, 2003, and the time for response is set from the September 10, 2003 mailing date of the replacement Office action.

The points raised in the Office action will now be addressed, beginning with the objection to the claims.

Section 112 Rejections

Claims 18 - 21 were rejected under 35 U.S.C. § 112, ¶ 1, as failing to comply with the written description requirement. The Examiner asserted:

> The specification never discloses a first cured adhesive polymer forming a spot situated in a middle region between the bump surface of the chip and the surface of the substrate, there being no first cured adhesive polymer at the contacts as claimed in claim 18.
>
> The specification never discloses a second cured adhesive polymer forming an underfill as claimed in claim 21.

These rejections are traversed.

Claim 18 recites "a first cured adhesive polymer forming a spot situated in a middle region between the bump surface of the chip and the surface of the substrate, there being no first cured adhesive polymer at the contacts." This feature is clearly shown, for example, at **24** in Fig. **1B**. It is described, for example, in the Brief Summary of the Invention at paragraphs [0005], [0010], and the Detailed Description of the Invention states, for example:

> A central area ... includes a spot of adhesive **24** small enough that it does not spread to the gold studs and the interconnection area during a subsequent bonding process.

(paragraph [0014]).

Claim 21 recites "a second cured adhesive polymer forming an underfill." This feature is described, for example, in the Brief Summary of the Invention at paragraph [0007], and the Detailed Description of the Invention at paragraph [0017] states:

> Overmolding fills the remaining space under the die and the space between the chips, resulting in a robust structure.

See also, paragraph [0019], describing wafer scale assembly, in which singulated substrate pieces each having a spot of the first adhesive are thermally bonded to accepted die on the wafer, and then the underfill is applied:

> After fully populating the wafer, the wafer is molded for underfilling and interchip space filling.

These rejections should be withdrawn.

Rejection under 35 U.S.C. §§ 102(b)

Claims 14 and 16 were rejected under 35 U.S.C. § 102(b) as being anticipated by Scharr *et al.* U.S. 5,346,857 ("Scharr"). The Examiner asserted:

> Regarding claim 14, Scharr et al. (figure 2) teach a chip (26) having bumps (28) formed thereon and a substrate (21) having interconnect points on a metallization (23) thereon, the bumps (28) forming contacts with the interconnect points, wherein an alloy (a region indicated by line [29]) is formed at an interface between the material of each bump (28) and the material of the metallization (23) in contact with the bump (28) (see figure 2; column 3, line 54 – figure, column 4, line 16).
>
> Re: claim 16, Scharr et al. teach the bump (28) material comprises gold and the interconnect points (metallization [23]) comprise Sn, and the alloy (a region indicated by line [29]) at the interface comprises a Au/Sn alloy (see figure 2; column 3, line 54 – column 4, line 16).

These rejections are traversed.

According to Applicants' invention, the interconnection is formed by contacting the bumps (14) on the die (12) with the interconnect points (18) on the substrate (16), and then applying heat for a limited time, sufficient to form an alloy of the bump material and the interconnect point material **in a layer (26) at the interface of each bump (14) and the corresponding interconnect point (18)**. For a Au-Sn junction, according to Applicants' invention a suitable temperature is about 232° C. and a suitable time is 1-2 seconds. At that temperature the Sn spots melt and, according to Applicants' specification, "the temperature at the bonding interface increases significantly, thereby dissolving some Au ... to create a bonding phase at the interface ... Preferably a 80%:20% Au:Sn alloy is formed at the interface". Applicants' Fig. 1B clearly shows that **the bonding phase (alloy) is limited to a layer 26 at the interface of the bump and the interconnect point**. The remainder of the bump is left substantially undisturbed by the process, and the bumps serve to maintain a standoff height between the die and the substrate during the bonding process.

Claim 14 is amended herein to more clearly define the structure of the interconnection between the bump and the substrate according to Applicants' invention.

In contrast, the Scharr process applies significantly higher heat for a significantly longer time, and Scharr expressly teaches that temperatures below approximately 280° C. are ineffective (Col. lines 33-35).

Particularly, regarding formation of the gold-tin alloy, Scharr states at Col. 3, lines 53-65:

> Gold bumps **28** are brought into contact with tin **23**. Pressure and heat are applied to the structure as described in FIG. **1** thereby forming a gold-tin alloy in the regions indicated by lines **29**.

The bonding scheme according to Scharr is as follows. The die is mounted in a top end effector, which includes a die tool whose temperature is maintained between approximately 200° C. and 250° C. (Col. 2, lines 28-36.) The substrate is mounted in a bottom end effector, which is heated by an infra-red heater. To form the interconnect, the gold bumped bond pads are contacted with the bonding areas on the circuit board; then the heater is ramped up to temperature between approximately 280° C. and 315° C. (Col. 3, lines 19-30.)

The temperature range is critical, according to Scharr:

> At temperatures below approximately 280° C., a gold-tin eutectic will not be formed, whereas at temperatures above approximately 315° C. the tin dissolves into the gold rather than forming a gold-tin eutectic alley. Thus, delamination occurs between the tin coating and any underlying conductive material.

Moreover, Scharr describes applying a compression load ranging between approximately 3 and 5 g per bump, for a time in excess of a range between 3 and 10 seconds. Because the heater is turned on prior to applying the load, and is turned off following the load period, Scharr teaches maintaining the high temperature régime for a time in excess of 3 to 10 seconds.

The **temperature régime described by Scharr promotes bulk melting of the Au-Sn eutectic composition and alloy formation in the bulk of the bump**, and can result in uncontrolled collapse of the bumps and degradation of the standoff height between die and substrate.

Accordingly, whatever may be meant by the "lines 29", Scharr does not teach an alloy **layer formed at an interface** between the bump and the material of the interconnect point, as in Applicants' invention as claimed. Moreover, far from suggesting such a structure, Scharr expressly teaches that a process for forming such a structure, as described in Applicants specification, will be ineffective to form an alloy as described by Scharr.

Accordingly, Scharr neither teaches nor suggests these features of applicants' invention, and the rejection for anticipation by Scharr should be withdrawn.

Rejection under 35 U.S.C. § 103(a)

Claim 15 was rejected under 35 U.S.C. § 103(a) for obviousness over Scharr in view of Nakamura *et al.* U.S. 6,326,234 ("Nakamura"). The Examiner acknowledged that Scharr does "not teach a cured adhesive polymer is situated in a middle region between the bump surface of the chip and the surface of the substrate", but asserts (referring to figure 4 of Nakamura) that "Nakamura teaches an adhesive polymer (7) is situated in a middle region between the bump surface of the chip (1) and the surface of the substrate (2)", and argued that it would have been obvious:

> to incorporate the teaching of Nakamura into the device taught by Scharr et al., because it provides good adhesion between the chip and the substrate.

This rejection is traversed. As explained above, Scharr does not teach the alloy layer according to Applicants' invention as claimed; and Nakamura cannot supply what Scharr lacks.

Moreover, Nakamura describes (*see*, Nakamura Fig. 4) a semiconductor device 10 in which the center of the gap 11 between the semiconductor chip 1 and the circuit board 2 is adhesively filled with a thermoplastic resin 7; and in which a peripheral portion of the chip is sealed by a curable resin 5 such as photocurable or thermosetting resin to form the semiconductor device 10. The thermoplastic resin works not to establish "good adhesion", but to provide for subsequent removal of the chip if the resulting assembly tests defective. Thus, it is essential in Nakamura that a **thermoplastic resin** be used in the center of the gap, as distinguished from a curable resin (Nakamura Col. 4, line 62 - Col. 5, line 12):

> In the conventional face-down type semiconductor device, the semiconductor chip and the circuit board are adhesively attached to each other and electrically coupled to each other by hardening the resin which is put between the semiconductor chip and the circuit board. Accordingly, since the curable resin is used, it is difficult to remove the semiconductor chip when the semiconductor chip is afterwards judged as a defective. However, according to the semiconductor device and the semiconductor device manufacturing method of the present invention, thermoplastic resin is used as temporarily fixing resin, and it is melted to temporarily couple the semiconductor chip and the circuit board to each other. When the semiconductor chip is judged as a defective in a subsequent check test, the semiconductor chip is heated to a temperature which is higher than the melting point or more of the thermoplastic resin to thereby easily remove the defective semiconductor chip from the circuit board.

Thus, Nakamura teaches away from using a curable resin in the center portion of the gap.

Applicants' claim 15 recites that a cured adhesive polymer is situated in a middle region between the bump surface of the chip and the surface of the substrate. No combination of Scharr and Nakamura teaches or suggests Applicants' invention and, accordingly, this rejection for obviousness should be withdrawn.

Claim 17 was rejected under 35 U.S.C. § 103(a) for obviousness over Scharr, the Examiner acknowledging that Scharr does "not explicitly teach the alloy at the interface is 20:80 Sn:Au alloy", but argues that it would have been obvious:

> for an alloy at the interface [to be] 20:80 Sn/Au alloy, says it has been held that discovering an optimum value of the results effective variable involves only routine skill in the art."

(citing *In re Boesch.*)

This rejection is traversed. Applicants have shown how to make an interconnect in which a low temperature and low pressure process is employed to obtain an alloy at the interface between the bumps and the interconnect points. As explained above, Scharr does not teach the alloy layer at the interface according to Applicants' invention as claimed. Moreover, Scharr expressly teaches away from attempting to make a Sn:Au eutectic using a temperature regime as taught by Applicants for making the alloy layer. In other words, no teaching or suggestion of Scharr can make a Sn/Au alloy (in any ratio) limited to a layer at the interface, because Scharr expressly teaches away from using a temperature regime by which such a structure can be obtained according to Applicants' invention.

Accordingly, it is submitted that neither Scharr nor Nakamura—nor any combination of Scharr and Nakamura—makes Applicants' invention. Accordingly, the rejections for obviousness should be withdrawn.

In view of the foregoing, it is believed that all the claims in the application are in condition for allowance, and action to that effect is requested.

This response is being filed, together with a Request for Continuing Prosecution, within the third month following the shortened statutory period set by the Examiner and, accordingly, it is accompanied by a petition for three months' extension of time and a fee or fee authorization therefor. The Commissioner is authorized to charge any additional fee[s] that may be required in connection with the filing of this paper, or to credit any overpayment, to Deposit Account 50-0869 (Order No. CPAC 1002-1).

If the Examiner determines that a conference would facilitate prosecution of this application, the Examiner is invited to telephone Applicants' representative, undersigned, at the telephone number set out below.

Respectfully submitted,

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